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Password Designing Using Programmable Logic Device (PLD)

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Abstract

Password can be applied as electronics key in security system. For example, it use to electronics key to wardrobe door or safety deposit box. This electronics key use the password code as a key that entered by the user to unlock the door. Base concept of Programmable Logic Device (PLD) is how to construct a programmable combinational logic circuit. The ability of PLD programming is planned at hardware level. PLD is a chip with high purpose to control the hardware base on it specification. PLD as digital logic IC can be change it functions using the programming language Hardware Description Language (HDL). The software that use is Warp 4.2 from Cyress. Using Personal Computer (PC), program logic or state diagram can be made by HDL using software text editor. HDL is compiled using software to make the logic circuit detail and produce the output of design that has been done. The circuit operation is simulated in NOVA checked the output of program suitable with user needed. PLD technology can be applied to password code with password code 527 to activated three output Y0,Y1 dan Y2.

Keywords : *Programmable Logic Device (PLD), Hardware Description Language (HDL), Password*

1 INTRODUCTION

Password is a word or string of characters used for user authentication to prove the identity or access to system, which must be kept secret from those not allowed access. Passwords are generally short, easy to remember and type. Password can be applied as electronics key in security system. For example, it use to electronics key to wardrobe door or safety deposit box. This electronics key use the password code as a key that entered by the user to unlock the door.

Programmable Logic Devices (PLD) technology is digital logic integrated circuit (IC) that can be changed the function using programming. Using PLD technology usesr can make own design and model that they want and need. It also can be reprogram and reconfigure the designing as user needed. Figure 1 shows how to built digital circuit using PLD easily. Base concept of Programmable Logic Device (PLD) is how to construct a programmable

combinational logic circuit. Combinational circuit is a circuit without memory device inside the system. The ability of PLD programming is planned at hardware level. In another word, PLD is a chip with high purpose to control the hardware base on it specification. By using unexpensive personal computer (PC), software program and a programmable logic devices (PLD) IC, a digital circuit can easily prototype. The five step process for creating a prototype using a PLD:

- Step 1 : Create the new circuit using the text editor or softwares schematic editor
- Step 2 : Compile the circuit into a bitstream file (file.jed) that when this file loaded into the PLD, will instruct it to act like the entered schematic
- Step 3 : Verify the operation of circuit using the softwares functional and timing simulator (NOVA)
- Step 4 : Download the circuit file from the PC to the PLD
- Step 5 : Physically test the PLD by activating its input and monitoring its output

This programmable logic prototyping method has the following advantages with manual wiring reduced to a minimum, prototypes can be constructed, tested, and modified at a much faster rate, wiring errors can be avoided, can experiment with many digital IC types without having to stock them, circuit design can be saved as electronic files within the PC and use again when needed, since the PLD can be used over and over, modificatons can be easily be made by altering the circuit in the PC and then downloading the new design into the IC of PLD.

Hardware Description Language (HDL) is a high-level programming language used to program a digital IC. It consists of a number of gates which can be programmed by disconnecting fuse inside the IC. Such as a programming language, HDL has its own rules in hierarchies or systematic program until the syntax used. HDL technology is classified by the number of existing gates. Programmable Logic Device (PLD) has less than 500 gates. A programming language that used is Warp 4.2 from Cyress. This software will produce a file with extension *.jed and can be downloaded to IC using IC programmer such as the All - 07, Easy Pro and others. Programming by using WARP 4.2 must obey the rules of programming that has been set by the vendor. Although programming language come from the different vendors but relatively the same because they use the reference to the international standard IEEE. General description of HDL programming technique can be seen in following explanation. There are two parts that must exist in programming:

1. Entity Declaration, entity declarations describe the input and output on the design of entity. It shows the values of the parameters. Entity declaration similar with the symbol scheme, which describes the relationship of component based design. Ports can be said to be a pin in the schematic symbol. Each port must have own name (identity), the direction (mode) and the clear type of data.
2. Architecture Body, Each architecture body integrated with an entity declaration. Architecture describes the contents of entity that declares an entity function also. If the entity declaration is displayed as a 'black box', which is the input and the output was

Table 1: Truth Table Design of Input dan Output Password

KODE	INPUT				OUTPUT		
PASSWORD	X1	X2	X1	X0	Y0	Y1	Y2
5	0	1	0	1	1	0	0
2	0	0	1	0	1	1	0
7	0	1	1	1	1	1	1

already known , while what is inside is not known , then the architecture that the contents of the black box that describes a function entity . There are three ways in architecture design, they are behavioral, dataflow, structural description atau mixing.

In this research is constructed the electronics key using Programmable Logic Device (PLD) technology using Hardware Description Language (HDL).

2 RESEARCH METHODOLOGY

The first step to design the password using PLD is design the program algorithm for HDL that familiar with stateCAD. The password for this study is three code digit 5, 2 and 7. Each digit consist of four biner bits are X0,X1,X2,X3 and in the system they have function as input. The outputs are coded as Y0,Y1 and Y2. If the combination of the password code that entered to the system is correct, then the output bit activated.

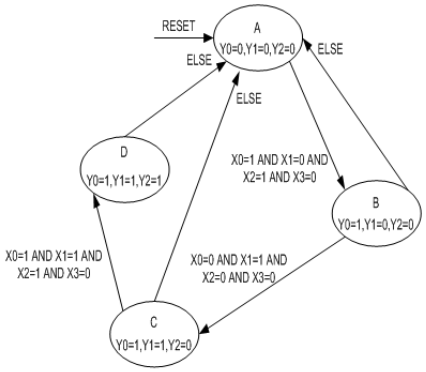

Figure 1: StateCAD diagram (Algorithm program) to Password "527"

The second step of this design constructs the circuit in Hardware Description Language (HDL) using text editor programming. In this case, the programming is used to substitute the function of circuit in programming language.

Listing program to Password using software WARP 4.2 with Hardware Description Language (HDL):

The circuit in program HDL form need to compile and change it becomes bitstream file with jed extension.

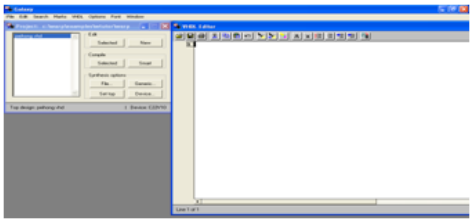

Figure 2: Text editor to typing the program

Declaring a Component (Device) and Entity Declaration
This part is declared the pin function in the password system, some pins as input and some are output.

```
use ieee.std_logic_1164.all;
entity peihong is
port (CLK,RESET,X0,X1,X2,X3: in std_logic;
Y0,Y1,Y2:out std_logic);
signal BP_Y0,BP_Y1,BP_Y2: std_logic;
end;
signal sreg : std_logic_vector (2 downto 0);
signal next_sreg : std_logic_vector (2 downto 0);
constant A : std_logic_vector (2 downto 0)  :="000";
constant B : std_logic_vector (2 downto 0)  :="001";
constant C : std_logic_vector (2 downto 0)  :="010";
constant D : std_logic_vector (2 downto 0)  :="011";
```

Achitecture_Body (Behavioral Description)
This part shows the procedure of passwords identifications. The output in HDL will active when the reset got the low input and clock active. This condition activated the output Y0, Y1 and Y2 trough the input X0,X1 and X2.

```
begin
process (CLK,RESET,next_sreg)
begin
if (RESET='1') then
sreg <= A;
elsif CLK='1' and CLK'event then
sreg <= next_sreg;
end if;
end process;
begin
process (sreg,BP_Y0,BP_Y1,BP_Y2,X0,X1,X2,X3)
BP_Y0 <= '0'; BP_Y1 <= '0'; BP_Y2 <= '0';
next_sreg<=A;
case sreg is
when A =>
BP_Y0<='0';
BP_Y1<='0';
BP_Y2<='0';
if (X0='1'and X1='0'and X2='1'and X3='0') then
next_sreg<=B;
else
```

The password design can be simulated using functional software and timming simulator, NOVA. The basic timming diagram is shown in figure 4 that have 4 inputs (X0,X1,X2,X3) and three outputs (Y0,Y1,Y2).

Figure 3: Compiling result for the password design

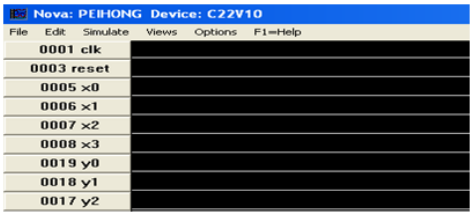

Figure 4: Basic timming diagram of NOVA

3 RESULTS AND DISCUSSION

The HDL programming for password design is simulated in NOVA software and got the result as shown in figure 5.

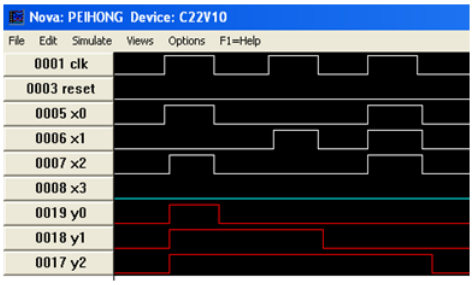

Figure 5: Timing diagram of password code simulations

The timing diagram shows the password input x0,x1,x2 and x3 and output y0, y1 and y2. Input code password 5 identical with biner 0101, input code password 2 idential with biner 0010 and input code 7 idential with biner 0111 and coded in x0, x1, x2 and x3. Input biner combination triggered the output y0, y1 and y2. In timing diagram, the first high clock have the value of x0 = 1, x1 = 0, x2 = 1 and x3 = 0 as biner combination of code password 5 and produced the combination of output y0 = 1, y2 = 0 and y3=0. The second high clock have the value of x0 = 0, x1 = 1, x2 = 0 and x3 = 0 as biner combination of code password 2 and produced the combination of output y0 = 1, y2 = 1 and y3=0. The third high clock have the value of x0 = 1, x1 = 1, x2 = 1 and x3 = 0 as biner combination of code password 7 and produced the combination of output y0 = 1, y2 = 1 and y3=1. It means, the first code

Table 2: Input and Output Password

KODE	INPUT				OUTPUT		
PASSWORD	X1	X2	X1	X0	Y0	Y1	Y2
5	0	1	0	1	1	0	0
2	0	0	1	0	1	1	0
7	0	1	1	1	1	1	1

activated the y0 output, second code for y1 and the last code for y2 output. Comparing with the password designing, the result show in the timing diagram has the same specification with designing as seen in the table below.

4 CONCLUSION

1. Programmable Logic Device (PLD) using programming language Hardware Description Language (HDL) can be a password.
2. The password in HDL is labeled input into X2, X1 and X0 with configuration 5 = 101b, 2 = 010b and 7 = 111b.
3. Code applied in this password is 527 to activated three outputs, 5 to Y0, 2 to Y1 and 7 to Y2.

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